

IN THE CLAIMS

Please cancel claims 11-15 without prejudice.

Please amend claim 60 as follows below.

The following is a listing of claims that replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1 1. (Original) A capacitor array in an integrated circuit,  
2 the capacitor array comprising:  
3 a plurality of dummy unit capacitor cells decoupled  
4 from signal paths to provide visual symmetry;  
5 a plurality of active unit capacitor cells having a  
6 terminal coupled to signal paths carrying analog signals;  
7 and  
8 wherein the plurality of active unit capacitor cells  
9 is arranged in the capacitor array with the dummy unit  
10 capacitor cells to provide visual symmetry and electrical  
11 symmetry.

1 2. (Original) The capacitor array of claim 1 wherein,  
2 the electrical symmetry to provide electrical matching  
3 between active unit capacitor cells, and  
4 the visual symmetry to provide process environment  
5 uniformity.

1 3. (Original) The capacitor array of claim 1 wherein,  
2 the visual symmetry is provided by  
3 selecting the same size and shape of capacitor  
4 plates for each unit capacitor in the capacitor array,  
5 and  
6 uniformly spacing each unit capacitor in the  
7 capacitor array;  
8 and wherein  
9 the electrical symmetry is provided by  
10 arranging the plurality of active unit capacitors  
11 amongst the plurality of dummy unit capacitors in the  
12 capacitor array so that the far range fringing fields  
13 are symmetric.

1 4. (Original) A capacitor array in an integrated circuit,  
2 the capacitor array comprising:  
3 a plurality of unit capacitor cells arranged to  
4 provide visual symmetry;  
5 a set of N active unit capacitor cells of the  
6 plurality of unit capacitor cells having a terminal coupled  
7 to a signal path to carry analog signals;  
8 if N is a prime number, arranging the N active unit  
9 capacitor cells to be symmetrically located to form an N-  
10 equilateral two-dimensional shape to provide electrical  
11 symmetry,  
12 otherwise if N is not a prime number,  
13 dividing the set of N active unit capacitor cells

14       into P subsets of M active unit capacitor cells,  
15       arranging the M active unit capacitor cells of each of  
16       the P subsets to be symmetrically located to form an  
17       M-equilateral two-dimensional shape in a neighborhood,  
18       and  
19             separating each neighborhood of each M-  
20       equilateral two-dimensional shape by one or more dummy  
21       unit capacitor cells to avoid encroachment of one  
22       neighborhood into another in order to provide  
23       electrical symmetry.

1   5. (Original) The capacitor array of claim 4 wherein,  
2       the plurality of unit capacitor cells are arranged in  
3       equally spaced apart rows and columns to provide visual  
4       symmetry.

1   6. (Original) The capacitor array of claim 4 wherein,  
2       the electrical symmetry to provide electrical matching  
3       between active unit capacitor cells, and  
4       the visual symmetry to provide process environment  
5       uniformity.

1   7. (Original) The capacitor array of claim 4 wherein,  
2       the N-equilateral shape is slightly skewed, and  
3       a predetermined distance of separation is maintained  
4       between active cells.

1 8. (Original) The capacitor array of claim 4 wherein,  
2 the unit capacitor cells are integrated circuit  
3 capacitors.

1 9. (Original) The capacitor array of claim 8 wherein,  
2 the integrated circuit capacitors are metal oxide  
3 semiconductor capacitors.

1 10. (Original) The capacitor array of claim 8 wherein,  
2 the integrated circuit capacitors are thin film  
3 capacitors.

1 11-15. (Cancelled)

1 16. (Original) A computer program product for layout  
2 of a capacitor array in an integrated circuit, comprising:  
3 a computer usable medium having  
4 computer readable program code to arrange a  
5 plurality of dummy unit capacitors and a plurality of  
6 active unit capacitors in a capacitor array to provide  
7 visual symmetry, and  
8 computer readable program code to arrange the  
9 plurality of active capacitors amongst the plurality  
10 of dummy unit capacitors in the capacitor array to

11 provide symmetric far range fringing fields to each of  
12 the plurality of active capacitors;  
13 and  
14 wherein the dummy unit capacitors are decoupled from  
15 signal paths and the active unit capacitors have at least  
16 one terminal coupled to a signal path carrying an analog  
17 signal.

1 17. (Original) The computer program product of claim  
2 16 wherein,  
3 the visual symmetry is provided by  
4 selecting the same size and shape of capacitor  
5 plates for each unit capacitor in the capacitor array,  
6 and  
7 uniformly spacing each unit capacitor in the  
8 capacitor array.

1 18. (Original) The computer program product of claim  
2 16 wherein,  
3 the computer usable medium further has  
4 computer readable program code to define the mask  
5 layers of a unit capacitor of the capacitor array.

1 19. (Original) The computer program product of claim  
2 16 wherein,  
3 the computer usable medium is a semiconductor medium,  
4 a magnetic medium, an optical medium, or a processor

5 readable medium.

1 20. (Original) The computer program product of claim  
2 16 wherein,  
3 the computer usable medium is a computer data signal  
4 embodied in a carrier wave over a transmission medium.

1 21. (Original) An N-bit digital to analog converter  
2 (DAC) with a binary-weighted capacitor ladder in an  
3 integrated circuit, the N-bit DAC comprising:  
4 N-1 sampling switches each having a control gate, a  
5 first pole, and a second pole coupled to a voltage  
6 reference;  
7 a switch controller to receive an N-bit digital data  
8 input signal and generate N-1 control signals, the N-1  
9 control signals respectfully coupled to each control gate  
10 of the N-1 sampling switches to switch the N-1 sampling  
11 switches open and closed in response to the N-bit digital  
12 data input signal;  
13 N capacitors formed out of a plurality of active unit  
14 capacitor cells in a capacitor array, each of the N  
15 capacitors having a top capacitor plate coupled together  
16 and to an output of the binary-weighted capacitor ladder,  
17 one of the N capacitors having a bottom capacitor plate  
18 coupled to a ground while the remaining N-1 capacitors have  
19 a bottom capacitor plate respectively coupled to each first  
20 pole of the N-1 sampling switches; and  
21 wherein the plurality of active unit capacitor cells

22 to form the N capacitors being arranged with a plurality of  
23 dummy unit capacitor cells in the capacitor array to  
24 provide visual symmetry and electrical symmetry.

1 22. (Original) The N-bit DAC of claim 21 wherein,  
2 the integrated circuit is a digital to analog  
3 converter.

1 23. (Original) The N-bit DAC of claim 21 wherein,  
2 the integrated circuit is an analog to digital  
3 converter and the N-bit DAC is a portion of each stage of  
4 the analog to digital converter to successively approximate  
5 the analog input signal.

1 24. (Original) The N-bit DAC of claim 21 wherein  
2 the electrical symmetry to provide electrical matching  
3 between active unit capacitors, and  
4 the visual symmetry to provide process environment  
5 uniformity.

1 25. (Original) The N-bit DAC of claim 21 wherein  
2 the visual symmetry is provided by  
3 selecting the same size and shape of capacitor  
4 plates for each unit capacitor in the capacitor array,  
5 and  
6 uniformly spacing each unit capacitor in the

7 capacitor array.

1 26. (Original) The N-bit DAC of claim 21 wherein  
2 the electrical symmetry is provided by  
3 arranging the plurality of active unit capacitors  
4 amongst the plurality of dummy unit capacitors in the  
5 capacitor array so that the far range fringing fields  
6 are symmetric.

1 27. (Original) The N-bit DAC of claim 21 wherein  
2 the electrical symmetry is provided by  
3 if a number M of active unit capacitor cells forming  
4 the capacitor is a prime number, arranging the M active  
5 unit capacitor cells to be symmetrically located to form an  
6 M-equilateral two dimensional shape to provide electrical  
7 symmetry,  
8 otherwise if M is not a prime number,  
9 dividing the set of M active unit capacitor cells  
10 into P subsets of Q active unit capacitor cells,  
11 arranging the Q active unit capacitor cells of each of  
12 the P subsets to be symmetrically located to form an  
13 Q-equilateral two dimensional shape in a neighborhood,  
14 and  
15 separating each neighborhood of each Q-  
16 equilateral two-dimensional shape by one or more dummy  
17 unit capacitor cells to avoid encroachment of one  
18 neighborhood into another.



1 28. (Original) The N-bit DAC of claim 21 further  
2 comprising:

3 N grounding switches each having a control gate, a  
4 first pole, and a second pole coupled to the ground;  
5 and

6 wherein one of the N grounding switches has the  
7 first pole coupled to the output;

8 wherein the remaining N-1 capacitors have their  
9 bottom capacitor plate respectively coupled to each  
10 first pole of the remaining N-1 grounding switches;  
11 and

12 wherein the switch controller to further generate  
13 N inverted control signals, the N inverted control  
14 signals respectfully coupled to each control gate of  
15 the N grounding switches to switch the N grounding  
16 switches open and closed in response to the N-bit  
17 digital data input signal.

1 29. (Original) An N-bit digital to analog converter  
2 (DAC) with an equally-weighted capacitor array in an  
3 integrated circuit, the N-bit DAC comprising:

4 a first plurality of N switches each having a switch  
5 control gate, a first pole, and a second pole, the second  
6 pole of each of the first plurality of N switches coupled  
7 to a low level voltage supply;

8 a second plurality of N switches each having a switch  
9 control gate, a first pole, and a second pole, the second

10 pole of each of the second plurality of N switches coupled  
11 to a voltage reference, the first pole of each of the  
12 second plurality of N switches coupled respectively to the  
13 corresponding first pole of the first plurality of N  
14 switches;

15 a digital input signal having N control signals, each  
16 of the N control signals coupled respectively to each  
17 switch control gate of the first plurality of N switches  
18 and coupled respectively to each switch control gate of the  
19 second plurality of N switches, the N control signals to  
20 switch the second plurality of N switches open and closed  
21 and to switch the first plurality of N switches closed and  
22 open, respectively, in response to the digital input  
23 signal;

24 N capacitors formed out of a plurality of active unit  
25 capacitor cells in a capacitor array, each of the N  
26 capacitors having a top capacitor plate coupled together  
27 and to an analog output of the DAC, the N capacitors each  
28 have a bottom capacitor plate respectively coupled to each  
29 first pole of the first plurality of N switches and each  
30 first pole of the second plurality of N switches; and

31 wherein the plurality of active unit capacitor cells  
32 to form the N capacitors being arranged with a plurality of  
33 dummy unit capacitor cells in the capacitor array to  
34 provide visual symmetry and electrical symmetry to provide  
35 a substantial equally matched capacitance for each of the N  
36 capacitors.

1 30. (Original) The N-bit DAC of claim 29 wherein,

2       the integrated circuit is a digital to analog  
3 converter.

1   31. (Original)       The N-bit DAC of claim 29 wherein,  
2       the integrated circuit is an analog to digital  
3 converter and the N-bit DAC is a portion of each stage of  
4 the analog to digital converter to successively approximate  
5 the analog input signal.

1   32. (Original)       The N-bit DAC of claim 29 wherein  
2       the electrical symmetry to provide electrical matching  
3 between active unit capacitors, and  
4       the visual symmetry to provide process environment  
5 uniformity.

1   33. (Original)       The N-bit DAC of claim 29 wherein  
2       the visual symmetry is provided by  
3       selecting the same size and shape of capacitor  
4 plates for each unit capacitor in the capacitor array,  
5 and  
6       uniformly spacing each unit capacitor in the  
7 capacitor array.

1   34. (Original)       The N-bit DAC of claim 29 wherein  
2       the electrical symmetry is provided by  
3       arranging the plurality of active unit capacitors

4        amongst the plurality of dummy unit capacitors in the  
5        capacitor array so that the far range fringing fields  
6        are symmetric.

1    35. (Original)        The N-bit DAC of claim 29 wherein  
2        the electrical symmetry is provided by  
3        if a number M of active unit capacitor cells forming  
4        the capacitor is a prime number, arranging the M active  
5        unit capacitor cells to be symmetrically located to form an  
6        M-equilateral two dimensional shape to provide electrical  
7        symmetry,  
8        otherwise if M is not a prime number,  
9        dividing the set of M active unit capacitor cells  
10       into P subsets of Q active unit capacitor cells,  
11       arranging the Q active unit capacitor cells of each of  
12       the P subsets to be symmetrically located to form an  
13       Q-equilateral two dimensional shape in a neighborhood,  
14       and  
15       separating each neighborhood of each Q-  
16       equilateral two-dimensional shape by one or more dummy  
17       unit capacitor cells to avoid encroachment of one  
18       neighborhood into another.

1    36. (Original)        The N-bit DAC of claim 29 wherein  
2        the first plurality of N switches are n-channel field  
3        effect transistors; and  
4        the second plurality of N switches are p-channel field  
5        effect transistors.

1 37. (Original) The N-bit DAC of claim 36 wherein  
2 the digital input signal is a thermometer coded  
3 digital input signal, and  
4 each of the N control signals are directly coupled  
5 respectively to each switch control gate of the n-channel  
6 field effect transistors and are directly coupled  
7 respectively to each switch control gate of the p-channel  
8 field effect transistors.

1 38. (Original) The N-bit DAC of claim 29 wherein  
2 the N control signals include N positive control  
3 signals and N negative control signals,  
4 each of the N positive control signals are directly  
5 coupled respectively to each switch control gate of the  
6 first plurality of N switches, and  
7 each of the N negative control signals are directly  
8 coupled respectively to each switch control gate of the  
9 second plurality of N switches.

1 39. (Original) The N-bit DAC of claim 38 wherein  
2 the N negative control signals are respective inverted  
3 logical signals of the N positive control signals.

1 40. (Original) The N-bit DAC of claim 29 further  
2 comprising:

3           a switch controller to receive the digital input  
4 signal and generate the N control signals in response  
5 thereto.

1   41. (Original)           The N-bit DAC of claim 40 wherein  
2           the N control signals include N positive control  
3 signals and N negative control signals,  
4           each of the N positive control signals are directly  
5 coupled respectively to each switch control gate of the  
6 first plurality of N switches, and  
7           each of the N negative control signals are directly  
8 coupled respectively to each switch control gate of the  
9 second plurality of N switches.

1   42. (Original)           The N-bit DAC of claim 41 wherein  
2           the N negative control signals are respective inverted  
3 logical signals of the N positive control signals.

1   43. (Original)           A pipelined analog to digital converter  
2 (ADC) in an integrated circuit to receive an analog input  
3 signal and to generate a digital output signal, the  
4 pipelined analog to digital converter (ADC) comprising:  
5           a plurality of M converter stages coupled in series  
6 together, each of the M converter stages to receive an  
7 analog input and generate an analog residue output, each of  
8 the plurality of M converter stages including  
9           a K-bit flash analog to digital converter to

10 receive the analog input and generate a stage digital  
11 output, wherein K is a variable from stage to stage  
12 over the plurality of M converter stages;

13 an N-bit digital to analog converter (DAC) with  
14 an equally-weighted capacitor array, the N-bit DAC to  
15 receive the stage digital output to generate an  
16 estimated analog output, the N-bit DAC including

17 a first plurality of N switches each having  
18 a switch control gate, a first pole, and a second  
19 pole, the second pole of each of the first  
20 plurality of N switches coupled to a first  
21 voltage reference,

22 a second plurality of N switches each having  
23 a switch control gate, a first pole, and a second  
24 pole, the second pole of each of the second  
25 plurality of N switches coupled to a second  
26 voltage reference, the first pole of each of the  
27 second plurality of N switches coupled  
28 respectively to the corresponding first pole of  
29 the first plurality of N switches,

30 wherein the stage digital output has N  
31 control signals, each of the N control signals  
32 coupled respectively to each switch control gate  
33 of the first plurality of N switches and coupled  
34 respectively to each switch control gate of the  
35 second plurality of N switches, the N control  
36 signals to switch the second plurality of N  
37 switches open and closed and to switch the first  
38 plurality of N switches closed and open,

39                    respectively, in response to the stage digital  
40                    output,  
41                    N capacitors formed out of a plurality of  
42                    active unit capacitor cells in a capacitor array,  
43                    each of the N capacitors having a top capacitor  
44                    plate coupled together and to the estimated  
45                    analog output, the N capacitors each have a  
46                    bottom capacitor plate respectively coupled to  
47                    each first pole of the first plurality of N  
48                    switches and each first pole of the second  
49                    plurality of N switches,  
50                    wherein the plurality of active unit  
51                    capacitor cells to form the N capacitors being  
52                    arranged with a plurality of dummy unit capacitor  
53                    cells in the capacitor array to provide visual  
54                    symmetry and electrical symmetry to provide a  
55                    substantial equally matched capacitance for each  
56                    of the N capacitors, and  
57                    wherein N is a variable from stage to stage  
58                    over the plurality of M converter stages;  
59                    and,  
60                    an analog subtractor to receive the analog input  
61                    and subtract the estimated analog output therefrom to  
62                    generate the analog residue output.

1    44. (Original)            The pipelined analog to digital  
2    converter (ADC) of claim 43 wherein  
3                    the analog subtractor includes an amplifier to amplify  
4    the magnitude of analog residue output.



1 45. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 wherein  
3 a first converter stage of the plurality of M  
4 converter stages to receive the analog input signal of the  
5 analog to digital converter (ADC) as the analog input,  
6 and the analog to digital converter (ADC) further  
7 includes  
8 a digital bit corrector to receive each stage  
9 digital output of the respective plurality of M  
10 converter stages and to generate the digital output  
11 signal of the analog to digital converter in response  
12 to the analog input signal.

1 46. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 further comprising:  
3 a last converter stage coupled in series with an Mth  
4 converter stage of the plurality of M converter stages, the  
5 last converter stage including  
6 an J-bit flash analog to digital converter to  
7 receive the analog residue output of the Mth converter  
8 stage as the analog input and generate a last stage  
9 digital output.

1 47. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 46 wherein  
3 a first converter stage of the plurality of M

4 converter stages to receive the analog input signal of the  
5 analog to digital converter (ADC) as the analog input,  
6 and the analog to digital converter (ADC) further  
7 includes  
8 a digital bit corrector to receive each stage  
9 digital output of the respective plurality of M  
10 converter stages and the last stage digital output of  
11 the last converter stage to generate the digital  
12 output signal of the analog to digital converter in  
13 response to the analog input signal.

1 48. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 wherein  
3 the N-bit DAC in each of the plurality of M  
4 converter stages further includes  
5 a switch controller to receive the digital  
6 input signal and generate the N control signals  
7 in response thereto.

1 49. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 wherein  
3 the first voltage reference is a negative voltage  
4 reference and  
5 the second voltage reference is a positive  
6 voltage reference.

1 50. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 wherein  
3 the first voltage reference is a low level  
4 voltage supply.

1 51. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 wherein  
3 the low level voltage supply is ground.

1 52. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 43 wherein  
3 the N-bit DAC in each of the plurality of M  
4 converter stages further includes  
5 a third plurality of N switches each having  
6 a switch control gate, a first pole, and a second  
7 pole, the second pole of each of the second  
8 plurality of N switches coupled to a low level  
9 voltage supply, the first pole of each of the  
10 third plurality of N switches coupled  
11 respectively to the corresponding first pole of  
12 the first plurality of N switches.

1 53. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 52 wherein  
3 the switch control gates of the third

4 plurality of switches are coupled together and to  
5 a reset control signal to close each of the third  
6 plurality of switches and initialize the N  
7 capacitors of the capacitor array.

1 54. (Original) A pipelined analog to digital converter  
2 (ADC) in an integrated circuit to receive an analog input  
3 signal and to generate a digital output signal, the  
4 pipelined analog to digital converter (ADC) comprising:  
5 a plurality of converter stages coupled in series  
6 together, each of the plurality of converter stages  
7 including  
8 a flash analog to digital converter to receive  
9 the analog input and generate a stage digital output;  
10 a digital to analog converter (DAC) with a  
11 capacitor array, the digital to analog converter to  
12 receive the stage digital output to generate an  
13 estimated analog output, the digital to analog  
14 converter including  
15 a plurality of switches each having a switch  
16 control gate, a first pole, and a second pole,  
17 a plurality of active unit capacitor cells  
18 in the capacitor array, each of the active unit  
19 capacitor cells having a capacitor plate coupled  
20 to each respective first pole of the plurality of  
21 switches, respectively,  
22 wherein the plurality of active unit  
23 capacitor cells to form the active capacitors  
24 being arranged with a plurality of dummy unit

25           capacitor cells in the capacitor array to provide  
26           visual symmetry and electrical symmetry to  
27           provide a substantial equally matched capacitance  
28           for each of the active unit capacitors.

1   55. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 54 wherein  
3       the electrical symmetry to provide electrical matching  
4   between active unit capacitors, and  
5       the visual symmetry to provide process environment  
6   uniformity.

1   56. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 54 wherein  
3       the visual symmetry is provided by  
4       selecting the same size and shape of capacitor  
5   plates for each unit capacitor in the capacitor array,  
6   and  
7       uniformly spacing each unit capacitor in the  
8   capacitor array.

1   57. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 54 wherein  
3       the electrical symmetry is provided by  
4       arranging the plurality of active unit capacitors  
5   amongst the plurality of dummy unit capacitors in the  
6   capacitor array so that the far range fringing fields

7           are symmetric.

1   58. (Original)           The pipelined analog to digital  
2   converter (ADC) of claim 54 wherein  
3           the electrical symmetry is provided by  
4           if a number M of active unit capacitor cells forming  
5   the active capacitor is a prime number, arranging the M  
6   active unit capacitor cells to be symmetrically located to  
7   form an M-equilateral two dimensional shape to provide  
8   electrical symmetry,  
9           otherwise if M is not a prime number,  
10           dividing the set of M active unit capacitor cells  
11   into P subsets of Q active unit capacitor cells,  
12   arranging the Q active unit capacitor cells of each of  
13   the P subsets to be symmetrically located to form an  
14   Q-equilateral two dimensional shape in a neighborhood,  
15   and  
16           separating each neighborhood of each Q-  
17   equilateral two-dimensional shape by one or more dummy  
18   unit capacitor cells to avoid encroachment of one  
19   neighborhood into another.

1   59. (Original)           The pipelined analog to digital  
2   converter (ADC) of claim 54 wherein  
3           a bottom capacitor plate is the capacitor plate of  
4   each of the active capacitors which is coupled to each  
5   respective first pole of the plurality of switches.

1 60. (Currently Amended) A pipelined analog to digital  
2 converter (ADC) in an integrated circuit to receive an  
3 analog input signal and to generate a digital output  
4 signal, the pipelined analog to digital converter (ADC)  
5 comprising:

6 a plurality of converter stages coupled in series  
7 together, each of the plurality of converter stages  
8 including

9 a flash analog to digital converter to receive  
10 the analog input and generate a stage digital output;

11 a multiplying digital to analog converter (MDAC)  
12 with a capacitor array, the digital to analog  
13 converter to receive the stage digital output to  
14 generate a residual analog output, the multiplying  
15 digital to analog converter including

16 a first plurality of switches each having a  
17 switch control gate, a first pole, and a second  
18 pole, the second pole of each of the first  
19 plurality of switches coupled together and to a  
20 negative reference voltage,

21 a second plurality of switches each having a  
22 switch control gate, a first pole, and a second  
23 pole, the second pole of each of the second  
24 plurality of switches coupled together and to a  
25 positive reference voltage, each first pole of  
26 the second plurality of switches correspondingly  
27 coupled to each first pole of the first plurality  
28 of switches, respectively, [[.]]

29           a third plurality of switches each having a  
30           switch control gate, a first pole, and a second  
31           pole, each second pole of the third plurality of  
32           switches corresponding coupled to each first pole  
33           of the first plurality of switches and each first  
34           pole of the second plurality of switches,  
35           respectively,

36           a fourth plurality of switches each having a  
37           switch control gate, a first pole, and a second  
38           pole, the second pole of each of the fourth  
39           plurality of switches coupled together and to an  
40           analog input,

41           a plurality of active capacitors in the  
42           capacitor array each having a first capacitor  
43           plate and a second capacitor plate, each first  
44           capacitor plate of the active capacitors coupled  
45           to each first pole of the third plurality of  
46           switches and each first pole of the fourth  
47           plurality of switches, respectively, each second  
48           capacitor plate of each of the active capacitors  
49           coupled together,

50           an operational amplifier having an input  
51           coupled to each second capacitor plate of each of  
52           the active capacitors, the operational amplifier  
53           to generate the analog residue output,

54           a switch having a switch control gate, a  
55           first pole, and a second pole, the first pole of  
56           the switch coupled to input of the operational  
57           amplifier and the second capacitor plate of each



58 of the active capacitors, the second pole of the  
59 switch coupled to the analog residue output of  
60 the operational amplifier, and  
61 wherein a plurality of active unit capacitor  
62 cells form the active capacitors and are arranged  
63 with a plurality of dummy unit capacitor cells in  
64 the capacitor array to provide visual symmetry  
65 and electrical symmetry to provide a substantial  
66 equally matched capacitance for each of the  
67 active capacitors.

1 61. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 60 wherein  
3 the multiplying digital to analog converter further  
4 includes  
5 a fifth plurality of switches each having a  
6 switch control gate, a first pole, and a second  
7 pole, the second pole of each of the fifth  
8 plurality of switches coupled together and to a  
9 low level power supply voltage, each first pole  
10 of the fifth plurality of switches  
11 correspondingly coupled to each first pole of the  
12 first plurality of switches and to each first  
13 pole of the second plurality of switches,  
14 respectively.

1 62. (Original) The pipelined analog to digital  
2 converter (ADC) of claim 61 wherein

3                   the low level power supply voltage is  
4                   ground.

1   63. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 61 wherein  
3       the multiplying digital to analog converter further  
4   includes  
5                   a sixth plurality of switches each having a  
6       switch control gate, a first pole, and a second  
7       pole, the second pole of each of the sixth  
8       plurality of switches coupled together and to the  
9       analog residue output, each first pole of each of  
10      the sixth plurality of switches coupled to each  
11      first capacitor plate of the active capacitors,  
12      each first pole of the third plurality of  
13      switches, and each first pole of the fourth  
14      plurality of switches, respectively.

1   64. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 60 wherein  
3       the electrical symmetry to provide electrical matching  
4   between active unit capacitors, and  
5       the visual symmetry to provide process environment  
6   uniformity.

1   65. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 60 wherein

3       the visual symmetry is provided by  
4             selecting the same size and shape of capacitor  
5       plates for each unit capacitor in the capacitor array,  
6       and  
7             uniformly spacing each unit capacitor in the  
8       capacitor array.

1   66. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 60 wherein  
3       the electrical symmetry is provided by  
4             arranging the plurality of active unit capacitors  
5       amongst the plurality of dummy unit capacitors in the  
6       capacitor array so that the far range fringing fields  
7       are symmetric.

1   67. (Original)       The pipelined analog to digital  
2   converter (ADC) of claim 60 wherein  
3       the electrical symmetry is provided by  
4       if a number M of active unit capacitor cells forming  
5   the active capacitor is a prime number, arranging the M  
6   active unit capacitor cells to be symmetrically located to  
7   form an M-equilateral two dimensional shape to provide  
8   electrical symmetry,  
9       otherwise if M is not a prime number,  
10       dividing the set of M active unit capacitor cells  
11   into P subsets of Q active unit capacitor cells,  
12   arranging the Q active unit capacitor cells of each of  
13   the P subsets to be symmetrically located to form an

14           Q-equilateral two dimensional shape in a neighborhood,  
15           and  
16                 separating each neighborhood of each Q-  
17           equilateral two-dimensional shape by one or more dummy  
18           unit capacitor cells to avoid encroachment of one  
19           neighborhood into another.